FULLY DIFFERENTIAL OPERATIONAL AMPLIFIER DESIGN USING INDIRECT AND NEGATIVE MILLER COMPENSATION

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Abstract- This paper presents the design and analysis of a fully differential operational amplifier (op-amp). The amplifier architecture is based on the two-stage op-amp architecture with compensation around each amplification stage. The design operates on a +3.3 V single-rail power supply voltage operation and has been designed using a 0.35 μm CMOS technology. The consideration in choosing the internal compensation method was based on analysis of the op-amp's frequency response and stability margins. To improve stability, indirect compensation is applied around the second stage of the amplifier architecture. To improve frequency response, negative Miller compensation is applied around the first stage with the aim to reduce the effect of the amplifier input capacitance. The other important influence on performance considered is temperature. The op-amp shows a better performance at lower temperatures whereas the performance reduces at higher temperatures.The design was simulated with a variation of temperature in the range of -40°C to 125°C. The validation strategy was based on simulation using typical, worst-case power andworst-case speed device models using the Cadence Spectre circuit simulator.

Index Terms- Fully differential,indirect compensation, negative Miller compensation, temperature.

I. INTRODUCTION

The fully differential op-amp is one possible type of op-amp structure producing a differential output signal as well as receiving a differential input signal. A fully differential amplifieris used in circuits such as filters, buffers, comparators, instrumentation amplifiers and oscillators. A fully differential op-amp is considered in this work and therefore has both differential inputs and outputs. The fully differential amplifier design is based on using a 0.35 μm CMOS (n-well) fabrication process. The design is based on the two-stage op-amp architecture, a structure typically employed to achieve a high output voltage swing and high DC gain.

In order to ensure stability when the op-amp is used in a negative feedback configuration [1], the op-amp frequency response should be internally or externally compensated in order to achieve both the required speed of operation and required margins of stability. Stability is typically provided for by using one of two compensation techniques. Firstly, direct (Miller) compensation and secondly, indirect Miller compensation. The direct compensation technique is based on negative feedback around the inverting op-amp output stage and requires a large value compensation capacitor in order to set the margins of stability in open-loop. It also produces a right-half plane (RHP) zero [2] in the system transfer function and thisis undesirable as it reduces the speed of op-amp. The other technique is indirect compensation [3, 4]. This technique improves the stability of anop-amp whilst requiring a smaller value compensation capacitor when compared to direct compensation. This allows the op-amp to achieve a high phase margin although it also reduces the unity gain frequency (UGF, f_t). The compensation capacitor (C_M) (Fig. 1) is connected to an internal low output impedance node from the first amplification stage [5]and theoutput of the second amplification stage. Moreover, it is used to avoid the right-half plane (RHP) zero and leads to an increase in the phase margin whilst requiring a small value compensation capacitor. Each compensation capacitance deals with stability and frequency response in addition to accounting for parasitic capacitances created by the capacitances within the transistors used. In addition, the poles created in the system transfer function by parasitic capacitances (and resistances) are major concerns in the design of analog integrated circuits. These need to be accounted for circuits such as the folded-cascode (FC) circuit as this circuit is usually chosen for high-frequency applications[6].

The UGF of the op-amp that uses a folded-cascode input stage is low as the folded-cascode is used to obtaina high DC gain but also increases the amplifier input capacitance (C_{in}) given by:

$$f_t = \frac{g_m}{2\pi C_{in}} \qquad (1)$$

C_{in} is the capacitance created by the transistors associated with the op-amp differential input terminals. Considering f_t is controlled by the op-amp input stage, the transconductance of the input transistor (g_m) is associated with the geometries of metal oxide semiconductor field effect transistor (MOSFET) used. Here, only one input transistor is noted as the differential input uses two identical transistors. An increase in g_m requires an increase in the transistor size. If the dimensions of the MOSFETs in the input stage are increased, the parasitic capacitances associated with the MOSFETs would

also increase. This increase has the effect of reducing the UGF.

Fig. 1 shows a block diagram view of the op-amp architecture considered in this paper. To reduce the effects of the parasitic capacitances, negative Miller compensation (C_{NM} in Fig. 1) is used around the input stage. A *negative capacitance* offers a method for reducing the effects of the transistor input capacitances by the partial cancellation of these capacitances [7].

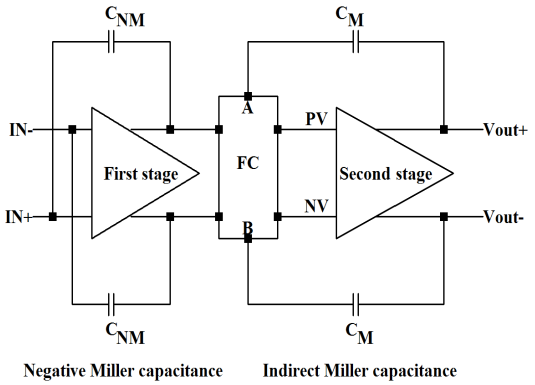

Fig.1. Block diagram of the fully differential amplifier design with compensation around each amplification stage

MOSFET performance is very much affected by change in temperature [8] with a decrease in its speed of operation due to a decrease in charge carrier mobility, as a result of a decrease in saturation velocities and an increase in junction capacitance values at higher temperatures. In addition, the MOSFET has a lower transconductance, lower bandwidth and lower threshold voltage [9] due to the decrease in the carrier mobility with increasing temperature.In this paper, section II will describe the two-stage CMOS fully differential op-amp design with rail-to-rail output designed using the Austria Mikro Systems (AMS) 0.35 μm CMOS (n-well) fabrication process. Section III will introduce indirect compensation and negative Miller compensation. Section IV will present simulation results for the design that uses a combination of indirect compensation and negative Miller compensation. In addition, the target amplifier operates on a +3.3 V single rail power supply. The op-amp operation was simulated using Cadence Spectre with typical, worst-case power and worst-case speed device models. Analysis of the circuit performance is provided in section IV. Section V provides conclusions to the paper and identifies future work.

II. OP-AMP ARCHITECTURE

The op-amp design considered in this work is based on the fullydifferential output (second) stage using a class-AB amplifier and a folded-cascode input (first) differential input stage.The full circuit schematic is shown in Fig.2. Fully differential amplifiers are commonly identified as DC-coupled, high-gain voltage amplifiers with differential inputs and differential outputs [10] and:

- The folded-cascode first stage is used as it provides for a high voltage gain.
- The class-AB amplifier is used in the second stage in order to achieve a large output swing range.
- Common mode feedback (CMFB) circuit.

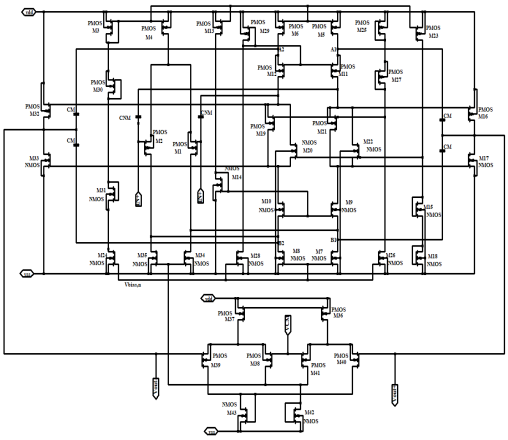

Fig.2. Fully differential op-amp circuit schematic

A. Differential Input stage (folded-cascode)

This section provides an analysis of the conventional fully differential folded-cascode structure whose circuit schematic is presented in Fig.1. The folded-cascode provides a large DC gain from a single amplification stage. Maximizing DC gain is achieved by creating a high-output impedance (output of the first stage).

The main concept of the folded-cascode op-amp design is to utilize cascode transistors of opposite type (i.e., nMOS rather than pMOS and vice-versa) from those used in the input stage [11] as shown in Fig. 3. In this work, transistors M1 and M2 are pMOS whereas cascode transistors M9 and M10 are nMOS. This type of connection provides a high resistance output node and the transconductance for the cascode is also nearly equal to the transconductance of the input pair [9]:

$$g_m = \sqrt{2I_D\left(\frac{K_p}{2}\right)\left(\frac{W}{L}\right)} \qquad (2)$$

$$W/L = \left(\frac{{g_m}^2}{2\,K_p\frac{I_D}{2}}\right) \qquad (3)$$

Where k_P is the transconductance parameter of the input stage transistor, I_D is the current flow through the input stage and W/L is the ratio of the input device width (W) and length (L). The theoretical formula for the UGF in Eq.1 is used to improve the UGF by increasing g_m. Increasing g_m is achieved by increasing the input transistor dimensions (W/L) (as shown in Eq. 3). This also coincides with the increase of the transistor parasitic capacitance values. It is however desirable to reduce the influence of parasitic capacitances of the input stage whilst maintaining a

high amplifier transconductance.A folded-cascode stage can be placed directly on the output of the input pair [12], the transistors M7 and M8 summing the differential currents of the input transistors. A high current results in a large transconductance. In addition, this gives the highest possible large frequency response as the gate capacitors of the nMOS transistors (M7 and M8) are smaller than that of the pMOS transistors. The pMOS transistors are usually chosen to be three times larger in order to compensate the g_m for the lower hole mobility in the pMOS transistor channel [12].

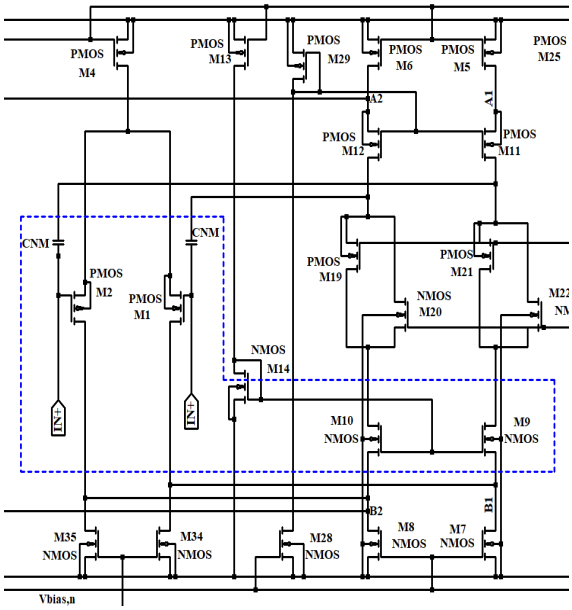

Fig.3. Differential input folded-cascode stage

B. Differential output stage (Class-AB stage)

The output stages are identified by transistors M16, M17 (positive node) and M32, M33 (negative node) in Fig. 2. The output is feedforward biased in class-AB by a mesh of head-to-tail connected transistors M21, M22, as shown in Fig. 3. The criteria utilized in the choice of the class-AB output stage implementation were [13]:

- A straightforward and high-speed design.
- No complex active or amplifier feedback paths in the class-AB control circuitry.
- Low-V_{DD} operation.
- Good power supply rejection ratio.
- No direct dependence on supply voltage for bias current setup.
- No noise or offset to be added to the first stage of the amplifier.

The schematic in Fig. 4 shows the implementation of the class-AB output stage integrated together with the first gain stage. The output signals of the first stage are supplied to the output stage at nodes *PV* and *NV*.

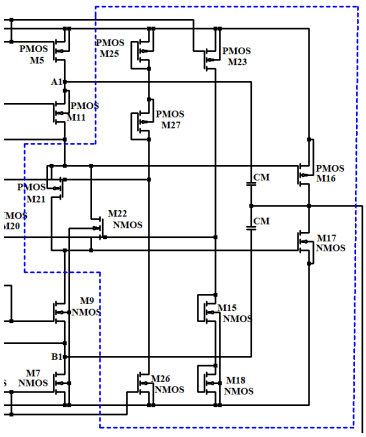

Fig.4. Half circuit of the op-amp showing the class-AB output stage

In normal circuit operation, M16 and M17 are biased in the conducting state (saturation). The voltages at nodes *PV* and *NV* are created to minimize the quiescent current through the large output driver devices, M16 and M17. This biasing arrangement is established within two translinear loops. The loop that biases M16 consists of M25, M27, M21, and M16. Likewise, M17 is biased by the loop consisting of M18, M15, M22, and M17.

C. Common mode feedback (CMFB)

A fully-differential topology requires the use of a *common-mode-feedback* (*CMFB*) circuit [14]. It controls the DC level of the voltages at the output terminals, Normally, the average of the op-amp outputs is called the common-mode output voltage. The two op-amp outputs swing around the common-mode voltage.

In this work, the CMFB stability improvement is achieved using split bias sources [15], as shown in Fig.5. It consists in decreasing the current bias ratio by splitting the bias current source controlled by the CMFB controlvoltage V_{CMFB}into two sources. The first source (M7-M8) is controlled by a fixed bias voltage $V_{bias,n}$and this provides a large current (for M28). The second source (M34-M35)(see Fig. 2) is biased by V_{CMFB}controlling the common-mode voltage at the op-amp output and provides the minimal required current I_{CMFB} *and* two split current sources in order to achieve stability of the CMFB loop [16]. The reduction of the bias current ratio reduces the DC gain and improve the pole to higher frequencies at the same time.

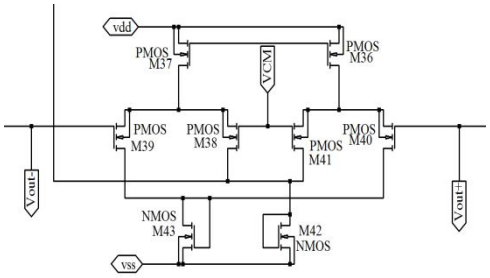

Fig.5. Common mode feedback circuit

III. STABILITY AND COMPENSATION

Phase margin (PM) is often used to define the stability of an op-amp. To achieve stability, the op-amp should have an open-loopPM of at least 45° at the UGF [17].When the op-amp is placed in a circuit design with negative feedback and under certain input conditions, the negative feedback becomes positive and the circuit output then oscillates. Compensation is used to improve the op-amp margin of stability in closed-loop and control the frequency response. The frequency compensation is a method for modifying the open-loop frequency response of the op-amp so that it behaves like single break response that provides sufficient positive PM [18]. A margin of stability has to be built-in to ensure stable operation under the required operating conditions in closed-loopto avoid oscillatory behavior. The designer can add a capacitance between specific nodes within the op-amp that deliberately reduces the open-loop gain magnitude at higher signal frequencies. This technique is referred to as *internal compensation.*

A. Indirect compensation

Indirect compensation is a way to compensate op-amps to enable higher speed operation [5]. In this technique, capacitors (C_M) are connected to an internal low impedance node (in Fig. 2, nodes *A1*, *A2*, *B1* and *B2*) in the first gain stage that permits indirect feedback of the compensation current from the output nodes (*Vout+* and *Vout-*) to the internal high-impedance node [19]. Indirect compensation allows for the use of a smaller compensation capacitor value since the load is relatively large. This compensation technique shifts the output pole to a frequency of approximately[20]:

$$\omega_{out} = \frac{C_M}{C_{GSOUT}} \frac{g_{mout}}{C_L} \quad (4)$$

Where $C_M$is theindirect compensation capacitor value and $C_{GS\,OUT}$ is the total gate-source capacitance value of the output transistor, g_{mout} is the total output transconductance as well C_L is the load capacitance. The small-signal model for the output stage of Fig. 4 is shown in Fig. 6. This model does not include any external load capacitance and resistance. Transistors M16, M17 and the current mirror M9, M10 in Fig. 4 provide the connection from one end of the compensation capacitor to the output and the other end of the capacitor to the drain of the current mirror device M7.The transfer function can be obtained by using a simplified small-signal model of one half of the output stage.

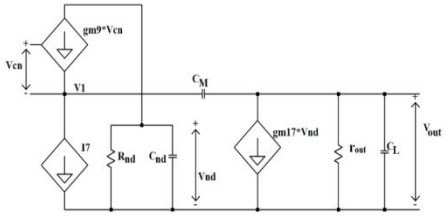

Fig.6. Half circuit of the output stage small-signal model [13]

R_{nd} represents the total resistance at the *NV* node and r_{out} represents the resistance at the output node. The current source M7 is represented by current I7 and the cascode drive transistor M9 is driven by its gate to source voltage *Vcn*. Current source I7 is the input signal current. Also, since node *V1* is a relatively low impedance node, it can be considered as a virtual AC ground. Therefore, the poles will be [13]:

$$p_1 \cong \frac{-1}{C_M \cdot R_{nd} g_{m-outn} R_{out}} \quad (5)$$

$$p_2 \cong \frac{-C_M}{C_{nd}} \cdot \frac{g_{m-outn}}{C_L} \quad (6)$$

P_2has increased by a factor of C_M/C_{nd}, which increases the UGF of the op-amp and hence increases the op-amp performance. Alternatively, to increase the slew rate, C_M can be decreased whilst maintaining the same UGF achievable with regular Miller compensation. Another positive result from this analysis is that no RHP zero results from this form of compensation. In a two stage op-amp employing indirect compensation, pole splitting is achieved with a lower value of the compensation capacitor (C_M) and with a lower value of second-stage transconductance ($g_{m\text{-}outn}$). This results in a higher UGF, with lower power consumption and a smaller layout, when compared with the direct Miller compensated op-amp [5].

B. Negative Miller compensation

The main drawback of the compensation around the second stage is the reduction the bandwidth because of additional capacitance. The effect of this capacitance in particular has to be considered at higher frequencies as it can produce unwanted phase shifts at higher frequencies that would not occur at lower frequencies. Another technique of compensation that can be used to decrease the effective capacitance of the input stage is by a parallel connection of a negative capacitance. The idea is shown in Fig. 1 and this can help to improve op-amp bandwidth. Negative Miller compensation is established on Miller effect [21], which describes the effect of the feedback capacitance C_{NM} on the input capacitance C_I. The two capacitors are connected through the non-inverting nets of the op-amp to partially cancel the effect of the transistor input capacitance.The effective input capacitance ($C_I^{'}$) is established at the input capacitance of a differential stage in Fig. 2. The equivalent input capacitance is given by:

$$C_I^{'} = C_I + (1 - |A|)C_{NM} \quad (7)$$

This creates the effect of a negative capacitance when the gain |A|is greater than unity. A negative capacitance property can therefore be utilized to improve bandwidth and phase margin. The negative capacitance design moves the non-dominant pole to a higher frequency whilst keeping the location of the dominant pole approximately the same [22].

IV. SIMULATION AND RESULTS

A fully differential amplifier was designed by combining two compensation techniques (indirect and negative Miller compensation). The circuit was simulated using Cadence Spectre. The threshold voltages are approximately 0.5 V and 0.7 V for nMOS and pMOS respectively. The op-amp was designed to operate on a +3.3 V single rail power supply voltage. Table I shows the frequency response analysis of the design based on typical device models. The design was simulated with no-load capacitance and load capacitances (C_L) of 0.1 pF, 0.5 pF and 1 pF. The capacitive load does not have an effect on the DC gain (84.9 dB). However, the load capacitance effect is noticeable as the signal frequency increases as shown in Fig. 7. At high frequency, the UGF varies from 707.97 MHz down to 505.23 MHz. In addition, the PM decreases with an increase in load capacitance value from the 77.90° down to 21.17°.Note that with this op-amp design approach, the PM reduces to below the considered minimum preferred value of 45° as the load capacitance increases. The other significant parameter is gain-bandwidth product (GBP) that is seen to be almost constant.

Table I. Open loop frequency response (typical device model)

Load capacitance (pF)	No load	0.1	0.5	1
DC gain (dB)	84.9	84.9	84.9	84.9
UGF (MHz)	707.97	693.03	588.04	505.23
PM (degrees)	77.90	65.38	28.91	21.17
GBP (MHz)	543.90	453.83	543.54	543.18

The op-amp design was then simulated at the process boundaries using the worst-case speed and worst-case power device models.

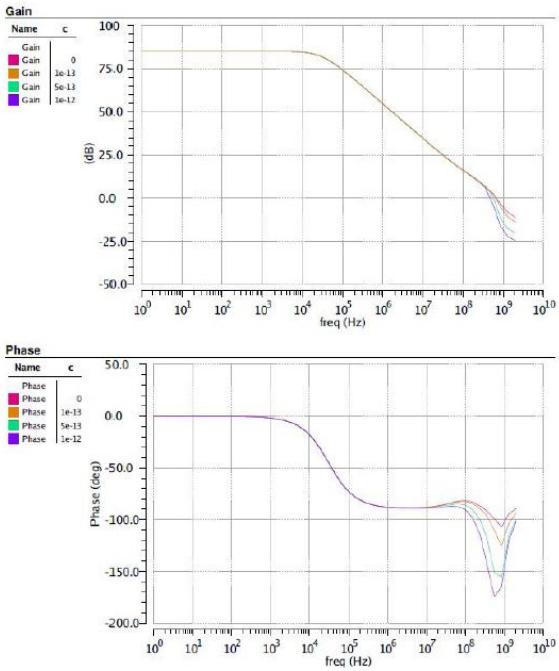

Fig.7. Open-loop frequency response for different load conditions (top) gain magnitude and (bottom) phase

The typical model means the nMOS and pMOS transistors have normal speed, worst-case speed means slow nMOS and slow pMOS transistors, and worst-case power means fast nMOS and fast pMOS transistors. Table II summarizes the frequency response and stability margins achieved with the different process variation models.

Table II. Frequency response with process variations (no output load)

Process	Typical model (TM)	Worst case power (WP)	Worst case speed (WS)
Gain (dB)	84.90	58.43	86.12
UGF(MHz)	707.97	2,146	143.1
PM (degrees)	77.90	44.74	85.77
GBP (MHz)	543.90	2,194	122.6

Over the temperature range from -40°C to 125°C, and with all system operating conditions, it can be seen that the temperature has a large influence on the circuit operation and hence changes the op-amp frequency response. Firstly, the operating temperature affects the frequency behavior of the open-loop gain magnitude curve, see Fig. 8. As the temperature varies, the open-loop gain magnitude varies between 84.9 dB and 50.71 dB in the typical model, worst-case power between 72.46 dB and 21.07 dB and the worst-case speed between 88.26 and 61.38 dB. The UGF is shown in Fig 9. It also changes with temperature. For the typical model, the UGF varies between 395 MHz and 465 MHz.Moreover, for worst-case speed, it varies between 31.1 MHz and 193 MHz. For worst-case power, the UGF varies between 2.56 GHz and 621 MHz.

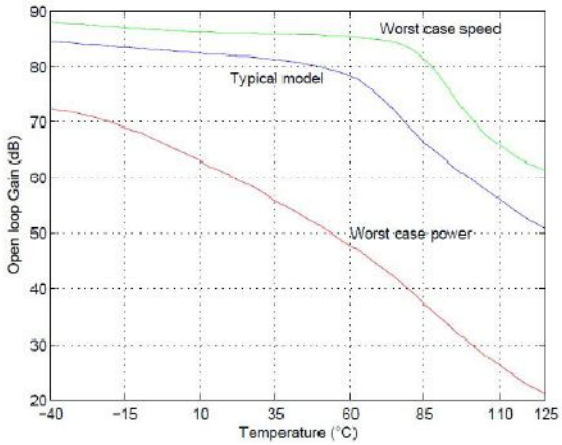

Fig.8. Open-loop gain versus temperature

Over the temperature range, as in shown in Fig. 10, the PM initially reduces as the temperature is increased from the minimum value However, as the temperature increases further, the PMs for the typical and worst-case power models change in reverse direction (increase instead of decrease). In the typical model case, the PM varies from 77.1° down to 62° and in the worst-case speed between 96.22° and 70.75°, but in the worst-case power, PM increases with increasing temperature from 49.13° to 82.64°.

As for the GBP, it can be seen that the largest change in performance is in the worst-case power model where it changes from 2.35 GHz to 623 MHz. Relatively small changes can be seen in worst case speed and typical model where the performance change from 26.6 MHz to 198 MHz and 497 MHz to 328 MHz respectively, as shown in Fig.11. The variation of performance with temperature is noticeably non-linear and for the typical and worst-case speed models, they initially show an increase when the temperature initially increases from its minimum value before reducing as the temperature reaches at 66° and 83° respectively.

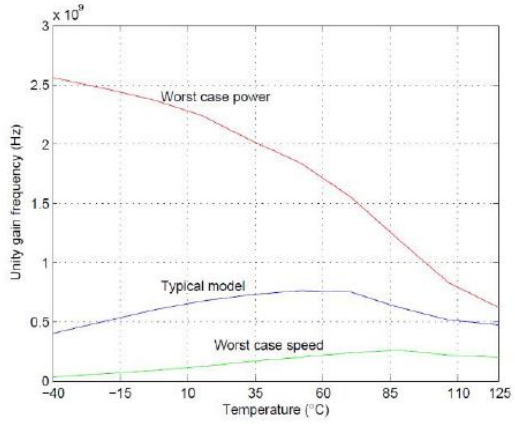

Fig.9. UGF versus temperature

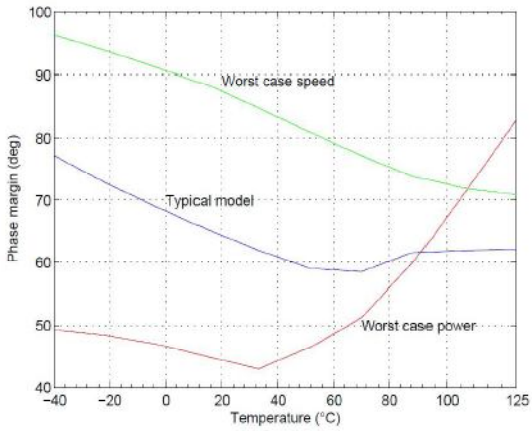

Fig.10. PM versus temperature

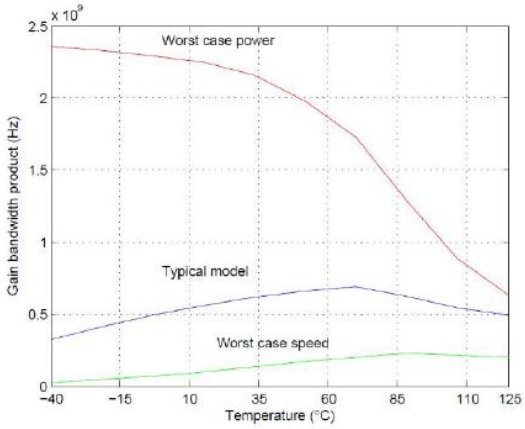

Fig.11. GBP versus temperature

CONCLUSIONS AND FUTURE WORK

In this paper, a fully differential two-stage op-amp design based on a folded-cascode input and class-AB amplifier output was presented. The design considered the proposed op-amp frequency response and stability control based on a combination of negative Miller compensation and indirect compensation. The design was based on a 0.35 µm CMOS fabrication process and its operation was validated through simulation using Cadence Spectre. The circuit design was developedin order to improve stability margins and frequency response with regard to PM, UGF and GBP. The circuit designed was analyzed at different operating temperatures and the simulation results show ~~a~~ deterioration in circuit performance with an increase in temperature. Future work will investigate this temperature related performance and the key circuit parameters that affect the frequency response of the op-amp over temperature.

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